Enhanced Transformer Differential Protection – Design, Test and Field Experience

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Abstract:

Transformer differential protection normally use dual slope or multiple slope characteristics to provide stability during through fault and load conditions. It also uses harmonic blocking criteria to provide stability during various transformer inrush conditions. The advancement in the materials used in transformers can cause a reduction in harmonics during a transformer inrush which can lead to reduced 2nd harmonic settings down to 10% or lower in some applications. This paper discusses the impact of a reduced 2nd harmonic threshold on the differential protection and highlights the benefits of waveform recognition algorithms such as the gap detection and the CT saturation techniques. These techniques are used to unblock the differential protection during internal faults, where CT saturation may lead to current waveforms that contain high levels of 2nd harmonic. It also highlights the benefits of an adaptive transient bias technique to provide high stability during through fault scenarios and includes results of extensive RTDS testing and some field performance examples.

1. Introduction

Traditional protection schemes use dual slope or multiple slope bias characteristics to provide stability during external faults with CT saturation, together with second harmonic as a restraining or blocking quantity for magnetising inrush conditions. However, studies have shown that there is a limitation with the dual slope characteristic for stability, to avoid requiring excessive over-dimensioning of the CTs. The second harmonic blocking has also been shown to slow down the differential protection for internal faults if CT saturation occurs. This is because CT saturated waveforms can also contain a high level of second harmonic component. Early studies on magnetising inrush currents indicate that the second harmonic content might be 15% or more of the fundamental current [3]. Recent studies indicate that improvements in the transformer design and core steel can result in a low content of second harmonic (as low as 7%) [3].

This paper highlights a novel transient bias technique for high stability during through faults combined with a no gap and CT Saturation recognition technique to unblock the differential protection during internal faults for faster clearance even in the presence of harmonics generated during CT saturation. A transient bias algorithm increases the operating threshold momentarily when there is a sudden increase in the bias current, thus enhancing stability during external faults. This approach has been optimised such that the performance during internal faults is not affected.

2. CT requirements and its impact on transformer differential protection

When applying high speed differential protection, it is important that the current transformers (CT's) should be capable of providing correct operating current to the relays. This means that the effect of primary fault currents containing transients must be understood and allowed for when choosing suitable CT's.

Primary fault currents contain a symmetrical a.c. component and an exponentially decaying d.c. transient component. The d.c. transient component is the more onerous from the point of view of C.T. saturation.

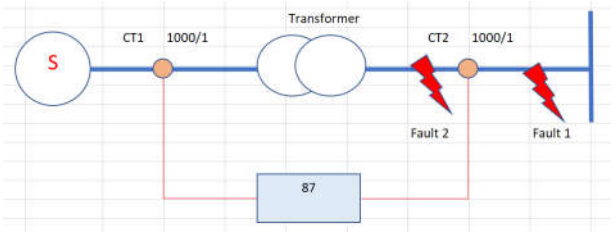


Figure 1

Figure 1 shows an example for transformer differential protection. To simplify this analysis, consider a transformer with a 1/1 transformation ratio and no phase shift. The response of CT_1 (current transformer 1) is used for analysing the impact on the differential protection. CT_2 is considered as an ideal CT. There are many technical literatures available on modelling of the current transformer, and it is not covered in this paper. The PSRC CT saturation calculator is one the best tools for analysing the CT behaviour. It is well known that the CT remanence, X/R ratio, knee point voltage, point on wave, total burden and fault current can cause saturation of a current transformer. While there is a need is to reduce the knee point voltage requirement, the impact of the remaining parameters must be evaluated for differential protection performance.

With reference to figure 1, considering a maximum through fault current of 40 kA with an X/R ratio of 80, to avoid CT saturation with no remanence, the CT_1 knee point voltage requirement can be calculated using (1+X/R)*(If/n)*(Rct+2Rl+Rb). Considering a CT_1 resistance of 2 Ω, lead resistance of 1 Ω and relay burden of 0.01 Ω, the ideal CT knee point voltage requirement is 12,992 V. This is almost impractical, and this paper evaluates the effect of reducing this requirement.

External fault condition: (Fault 1 in figure 1)

Consider case 1 with a knee point voltage of 12992 V for CT_1. For the through fault current of 40 kA, the secondary current available to the relay (assuming no remanence) is as shown in figure 2.

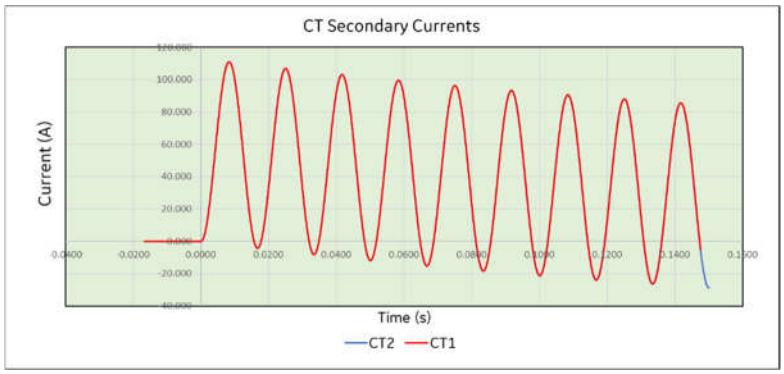


Figure 2

As the knee point of CT_1 is calculated to avoid CT saturation, the CT_1 and CT_2 (Ideal CT) currents are almost exactly matching each other. Therefore, this results in a low differential current with a very high value of bias current. The impact of the steady state ratio error is also ignored to analyse the transient response of the current transformers on the differential protection.

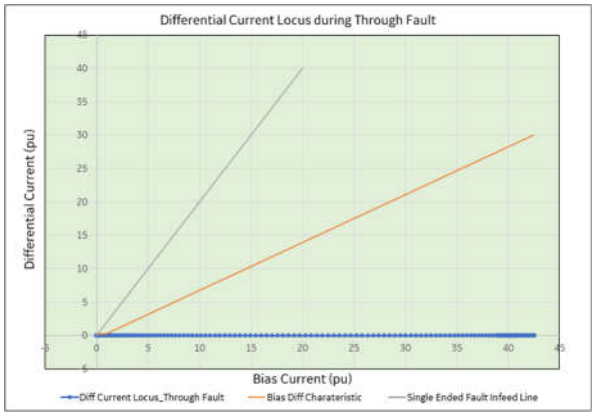


Figure 3

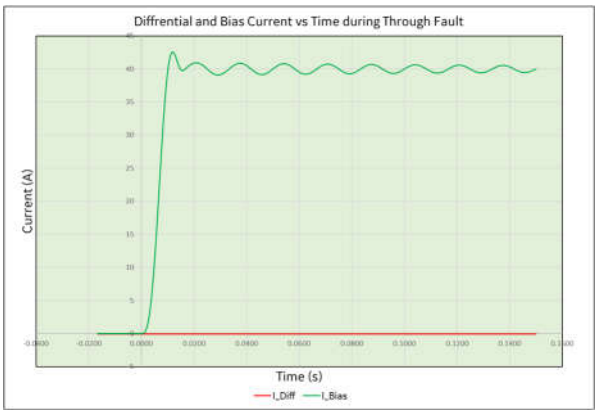
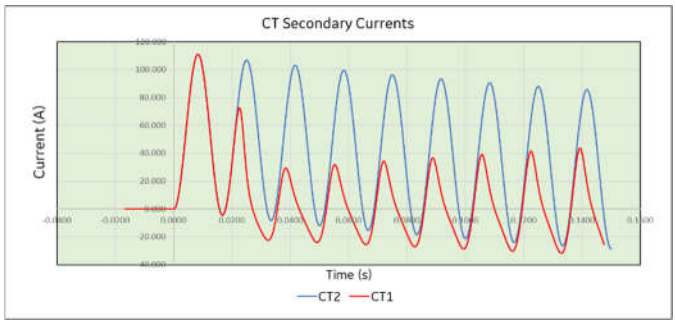


Figure 4

Figure 3 shows the differential current locus during the through fault (Fault 1). Note that the differential current locus remained in the restraining region during the entire duration of the fault. Figure 4 shows the differential and bias current against time. It shows the rise in bias current with no change in the differential current.

Case 2 considers the impact of reducing the knee point voltage of CT_1 to 10% of the ideal value (1299.2 V) and maintaining all other parameters the same as case 1. Figure 5 shows the CT_1 and CT_2 currents during the through fault (fault 1).



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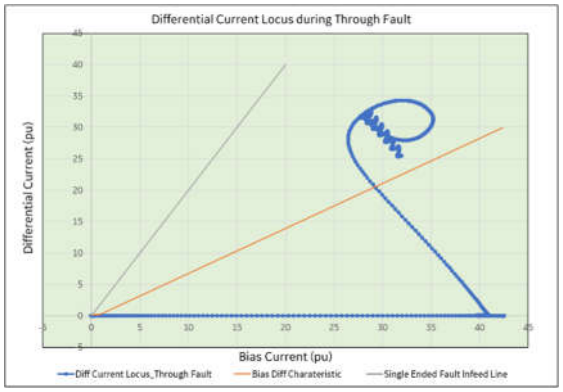

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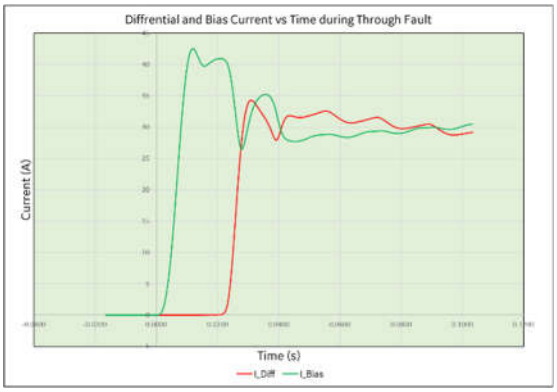

Figure 7

Figure 6 shows that as the CT_1 goes into saturation, the differential current locus moves to the operating region. Figure 10 shows the rise in both bias and differential current during the external fault with CT saturation. As seen in figure 7, the bias current rises before the differential current and can be used to indicate the external fault condition.

Case 3 reduces the knee point voltage of CT_1 to 1% of the ideal value (129.92 V) and maintains all other parameters the same as case 1. Figure 8 shows the CT_1 and CT_2 currents during the through fault (fault 1). The differential current locus of figure 9 shows that as the knee point voltage is reduced, the differential current locus moves closer to the single ended fault infeed line and takes a significantly longer time to move to the restraining region. Figure 10 shows the reduction in time between the rise of the bias and differential current during the through fault.

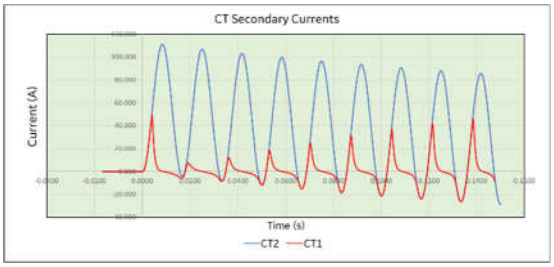

Figure 8

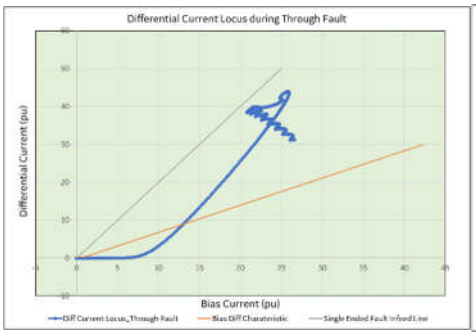

Figure 9

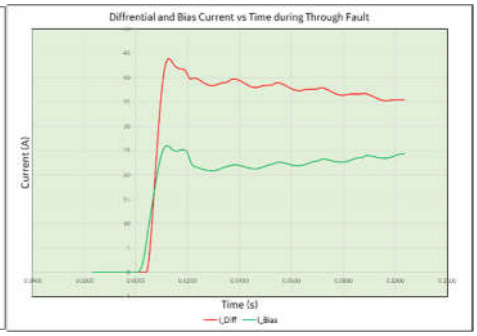

Figure 10

For all cases considered so far for through faults, the differential current locus crosses the slope 2 as the through fault current was kept constant at 40 kA.

Case 4 considers the knee point as the same as case 3 and the application of load on the transformer. As seen in figure 11, a reduced CT Knee point voltage can also cause saturation of the current transformers during application of load on the transformers. The differential current locus is crossing the bias characteristic for slope 1 (as shown in figure 12) and moves into the restraining region as the CT_1 comes out of saturation.

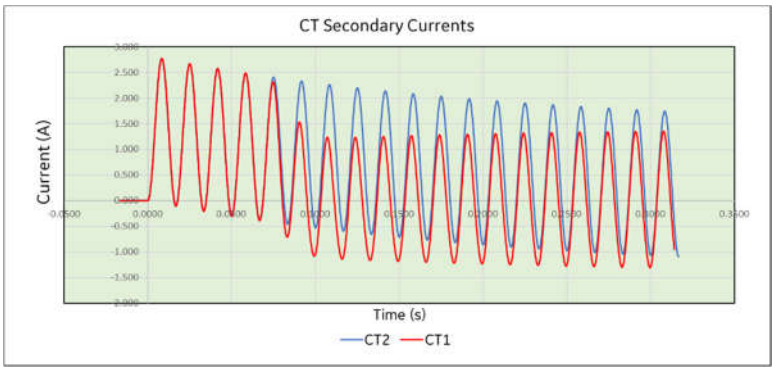

Figure 11

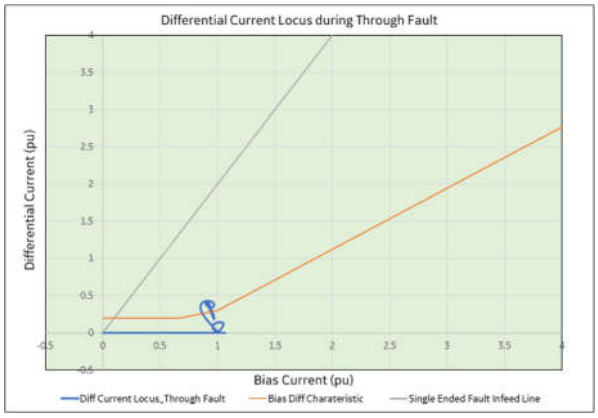

Figure 12

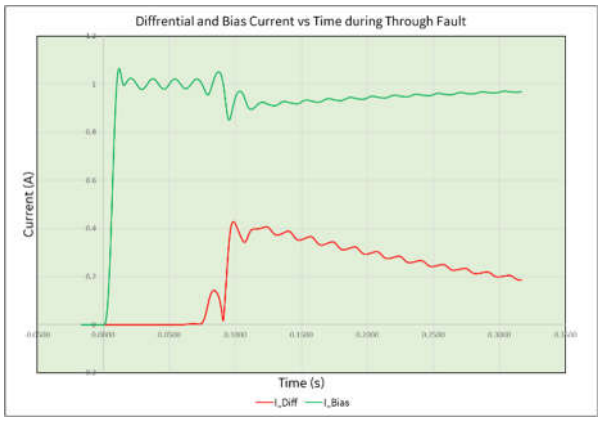

Figure 13

From the through fault and load cases discussed above, it is observed that CT saturation causes the differential current locus to move into operating region. How far it will move into operating region and when it will come out from the operating region (to the restraining region) is dependent upon the level of saturation and the primary & secondary time constants. It also shows that the multi slope characteristic may not be suitable in case of reduced CT knee point voltage and an additional biasing technique is needed.

<u>Internal fault condition: (Fault 2 in figure 1)</u>

Similar to through fault cases, internal faults (Fault 2) are investigated with the ideal CT knee point voltage (Vk), 10 % of the ideal Vk, and 1% of ideal Vk.

Figure 14 shows the secondary current output of CT_1 for an internal fault with an ideal knee point voltage. It also shows the 2nd harmonic component in the waveform. If the relay is set to block the differential element for a 2nd harmonic above 15% of the fundamental value, as seen in figure 14 the 2nd harmonic component in the waveform drops below the set threshold in a very short time, less than one cycle for 60 Hz. Figure 15 shows the 2nd harmonic component, its' threshold and the blocking signal above the set value.

Note: The 2nd harmonic component is often used to identify magnetising inrush conditions.

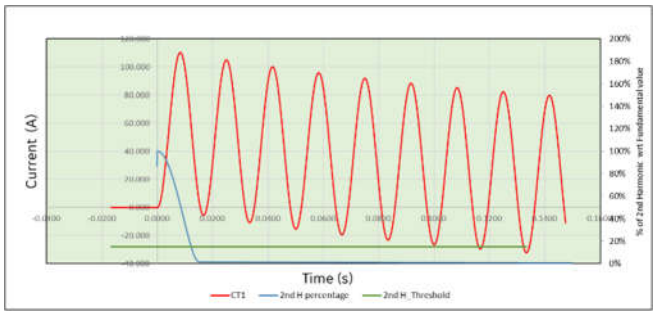

Figure 14

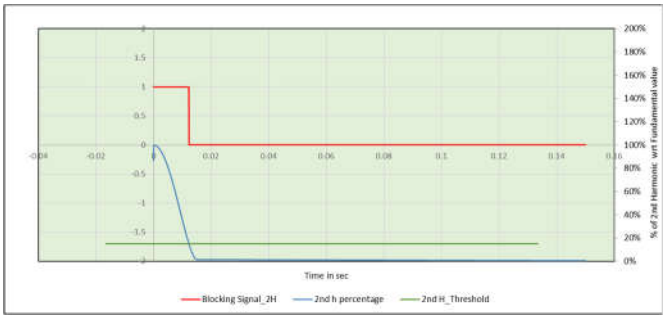

Figure 15

Figure 16 shows the differential current locus for fault 2 and it is aligned with the single ended fault infeed line. The differential and bias current over time is shown in figure 17 and as seen, the differential current rises before the bias current during an internal fault.

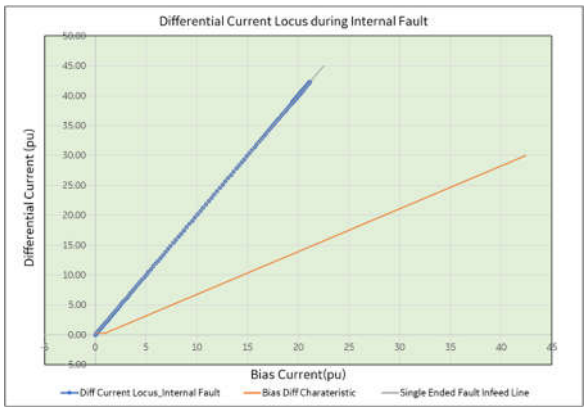

Figure 16

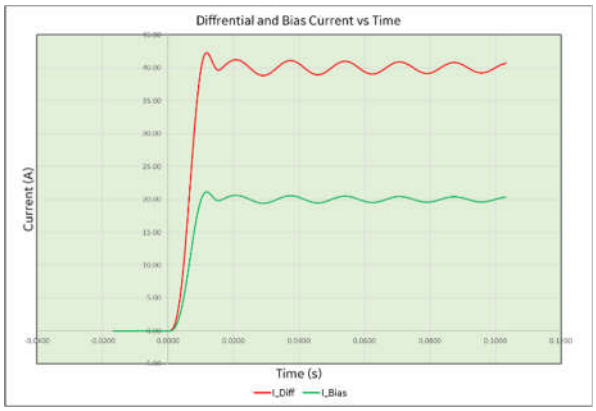

Figure 17

Figure 18 shows the secondary current output of CT_1 for an internal fault with the knee point voltage of 10% of the ideal value. It also shows the 2nd harmonic content in the waveform and the set 2nd harmonic threshold. It is seen that the 2nd harmonic content remains below the set value for a very short duration of time.

Figure 19 shows the 2nd harmonic blocking signal used for the biased differential element and it was low only for a very short duration of time. The differential relay should operate for such cases and isolate the fault. However, this time may not be sufficient to allow the differential protection to operate.

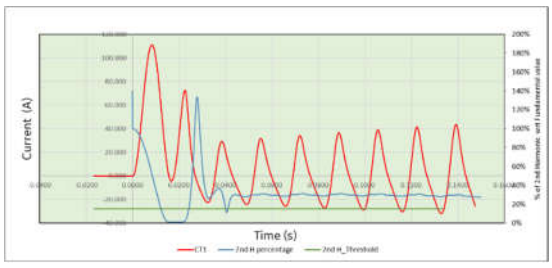

Figure 18

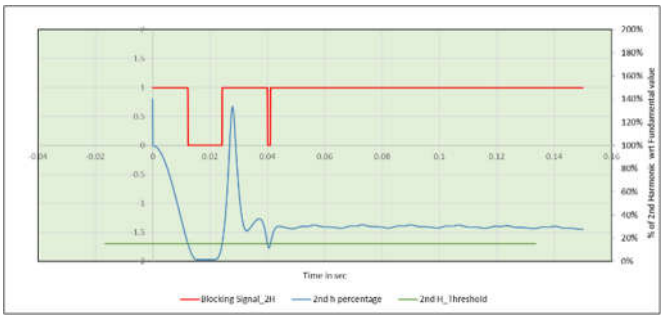

Figure 19

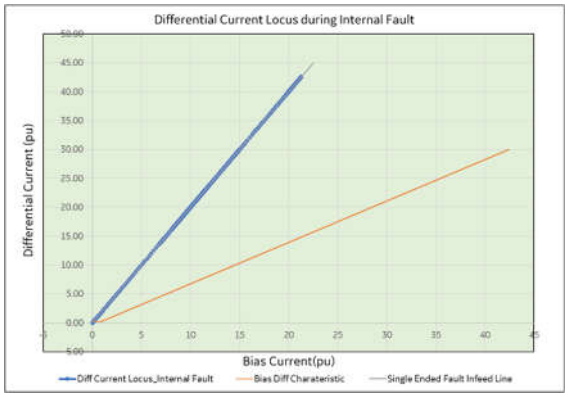

Figure 20

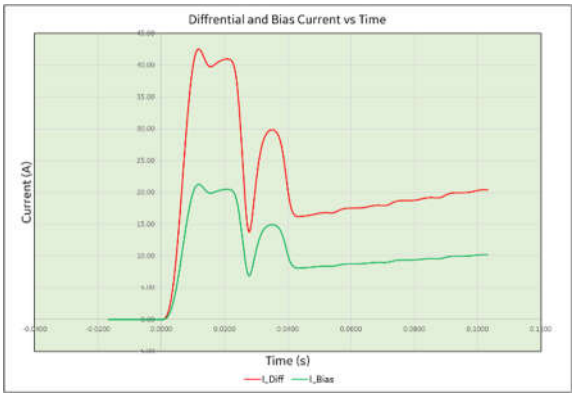

Figure 21

Figure 20 shows the differential current locus and it remained on for the single ended fault infeed line. From figure 21, it is evident that even during an internal fault with CT saturation, the differential current rises faster than the bias current.

Figure 22 shows the CT_1 current waveform during an internal fault with the knee point voltage of 0.1 % of the ideal value (129.92 v). As seen in the waveform, the saturated waveform is rich in harmonics and the blocking signal remained active during the entire duration and could prevent the operation of biased differential element.

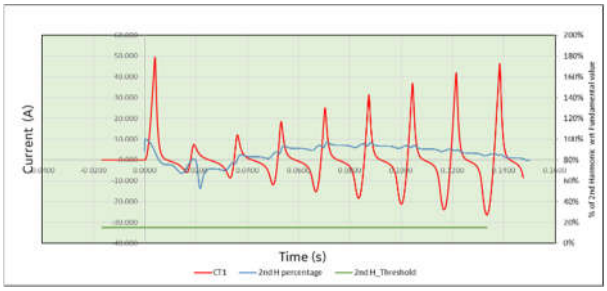

Figure 22

Figure 23

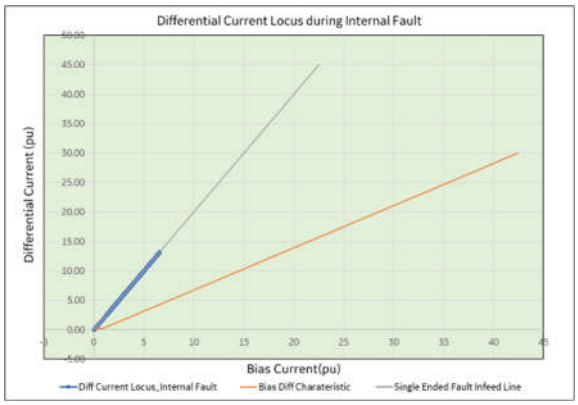

Figure 24

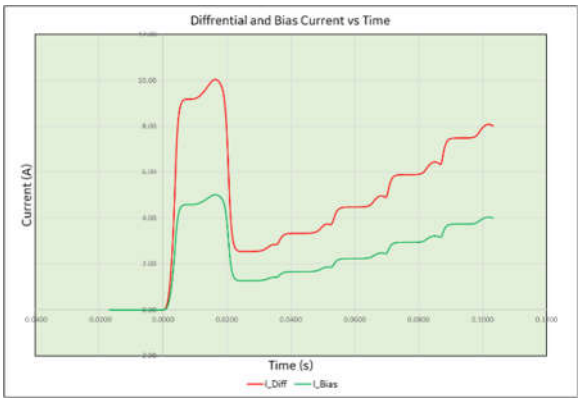

Figure 25

As seen in figure 24 and 25, even though the differential current locus is in the operating region the blocking signal generated due to the 2nd harmonic can prevent operation of the biased differential element. For all cases considered so far for an internal fault, the fault current was 40 kA.

The fast unrestrained element (highset) can operate for some of internal faults if the differential curent during the internal fault is above the setting of the unrestrained element. The unrestrained element is generally set above the maximum through fault current or inrush current whichever is greater to prevent operation during through fault or transformer energisation. As the CT1 and CT2 ratio used for analysis is 1000/1 A, an inrush current of 8000 A (8 pu) is considered. Figure 26 shows the CT1 secondary current for an internal faut with a fault current of 7 kA. With a reduced knee point voltage of 129.92 V, the CT1 secondary current during an internal fault with an X/R ratio of 20 is shown in figure 26.

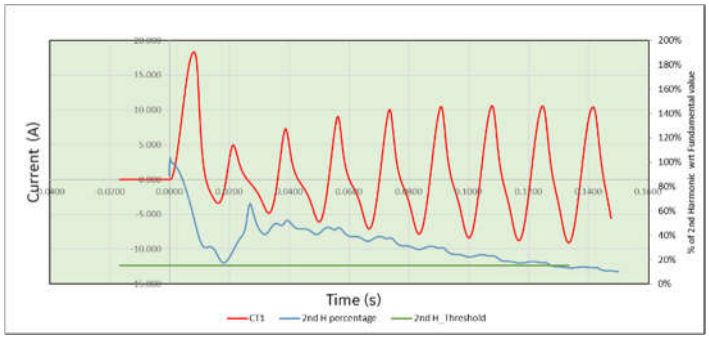

Figure 26

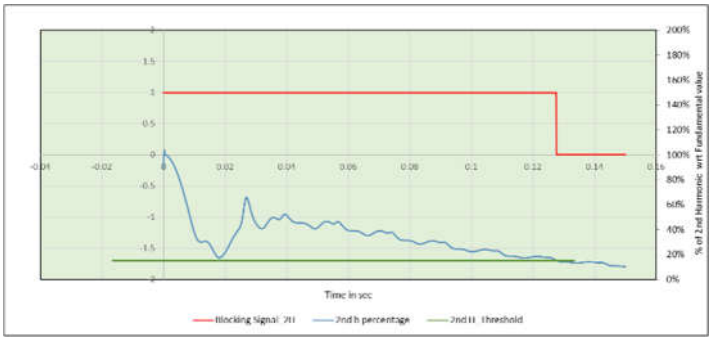

Figure 27

Figure 26 and 27 shows the harmonic content against the set 2nd harmonic threshold. As seen in figure 27, the 2nd harmonic content drops below the set value of 15% after 120 ms following the fault inception. Figure 28 shows that the differential current locus in the operating region for the entire duration, and from figure 29 it is clear that the differential current can remain below the unrestrained (highset) element during heavy CT saturation for an internal fault.

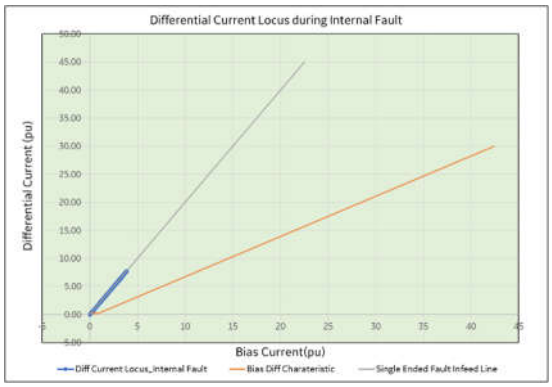

Figure 28

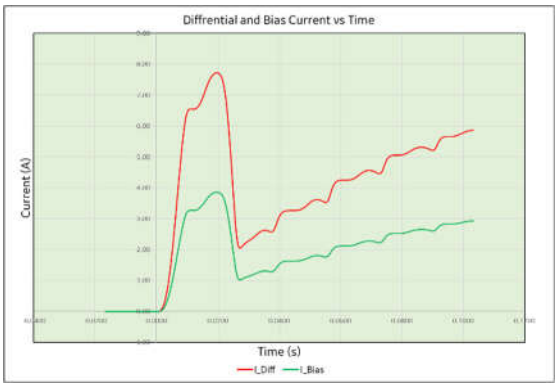

Figure 29

Considering the cases discussed for internal faults, it is evident that as we reduce the CT knee point voltage, it can cause saturation of the CT's and thereby produce higher 2nd harmonics. To overcome this difficulty and provide faster fault clearance, a method to unblock the biased differential element in the presence of higher 2nd harmonics is needed.

3. Improving stability of biased differential element during through faults

To provide further stability for external faults, additional measures are considered for the calculation of the bias current, such measures include: delayed bias, maximum bias and transient bias.

The delayed bias is calculated on a per phase basis and it is the maximum of the fundamental bias quantities calculated within the last cycle. The delayed bias provides added stability when an external fault is cleared and the fault currents drop off.

Ibias A_delayed = Maximum [Ibias,A(n), Ibias,A (n-1),Ibias,A (n – (k-1))] (1)

Ibias B_delayed = Maximum [Ibias,B(n), Ibias,B (n-1),Ibias,B (n – (k-1))] (2)

Ibias C_delayed = Maximum [Ibias,C(n), Ibias,C (n-1),Ibias,C (n – (k-1))] (3)

The maximum bias is the maximum of the delayed bias currents from all three phases. The maximum bias is used to prevent maloperation under external faults conditions, when spill current could flow into the CT of a healthy phase, if the CT is partially saturated.

Ibias,max = Maximum [IbiasA_delayed, Ibias,B_delayed, Ibias,C_delayed] (4)

The maximum bias is used to calculate the differential operating current Iop. The following equations define the operating characteristic (considering the multiple slopes of the bias characteristic).

Characteristic equation for range:

$$0 \le I_{bias,\max} \le \frac{I_{s1}}{K_1} \quad (5)$$

$$\mathrm{Iop} = \mathrm{I_{s1}} \quad (6)$$

Characteristic equation for range

$$\frac{I_{s1}}{K_1} \le I_{bias,\max} \le I_{s2} \quad (7)$$

$$Iop = K_1 \cdot I_{bias,\max} \quad (8)$$

Characteristic equation for range:

$$\mathrm{I_{bias}} \ge \mathrm{I_{s2}} \quad (9)$$

$$Iop = K_1 \cdot I_{s2} + K_2\left(I_{bias,\max} - I_{s2}\right) \quad (10)$$

K_1: characteristic slope in range (11)

K_2: characteristic slope in range (12)

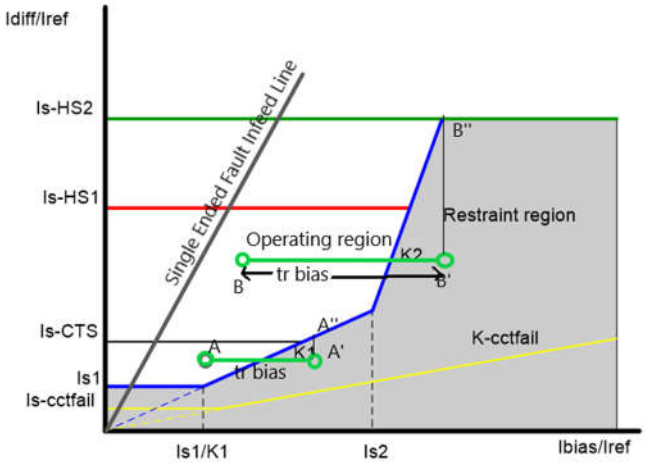

Figure 30 Tripping characteristic of differential protection

The transient bias is introduced when there is a sudden increase in the mean bias measurement and the external fault detector is activated. As shown in figure 30, point A is without transient bias and the transient bias moves the point to A' in the restraining region. Figure 30 also shows that depending upon the position of the differential point in the operating region for an external fault (point A or B), a different value of transient bias is added. As the differential point A and B moves to the restraining region, it requires a higher value of differential current (additional A'-A'' and B'-B'') for the operation of the differential element.

The external fault detection technique considers the time to saturation. On occurrence of an external fault the bias current changes but the differential current only increases after the CTs saturate. The external fault detection algorithm is on a per phase basis. Once the transient bias is introduced, it decays exponentially and resets to zero once the relay trips, or if the transient bias quantity is below the differential operating current threshold Is1. A phase comparison algorithm is also used to reset the transient bias during some evolving fault conditions. The operating current threshold is calculated at the maximum bias current. The transient bias is calculated on a per phase basis and is added to the operating current calculated at the maximum bias. Therefore, the following differential current thresholds are calculated:

Diff threshold phase A = Iop at (max bias + transient bias)_phase A (13)
Diff threshold phase B = Iop at (max bias + transient bias)_phase B (14)
Diff threshold phase C = Iop at (max bias + transient bias)_phase C (15)

The differential current is compared against the differential current threshold given above on a per phase basis. If the differential current is above the threshold, the biased differential element will trip as long as the second harmonic and fifth harmonic blocking elements are not asserted.

The transient bias technique considers a decay time constant, stability coefficients and the differential function settings to provide a dynamic bias characteristic.

Figure 31 shows the results of RTDS testing and differential current thresholds calculated by the relay on a per phase basis for a phase A-N external fault on the star side of a Ynd11 transformer. From figure 31, it is evident that the transient bias has increased the differential current threshold for an external fault.

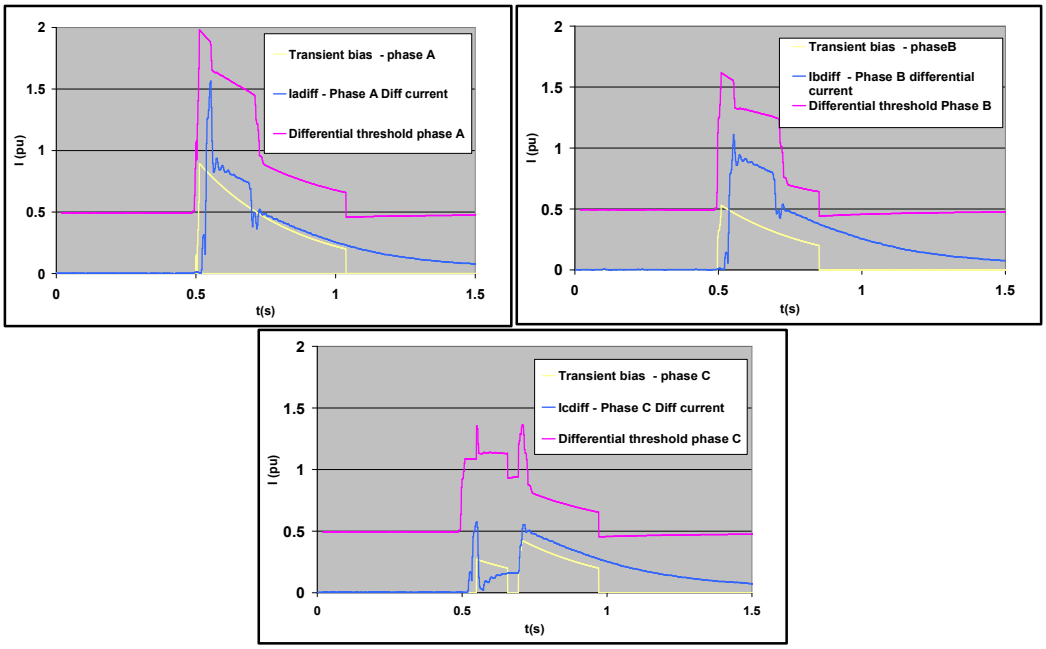

Figure 31 Transient bias – external fault

Figure 32 shows differential current locus, nominal characteristic (conventional multislope characteristic) and the change in the differential current threshold due to the transient bias during an A-N external fault. As shown in figure 32, the differential current locus during an external fault traversed from A→B→C and was in the operating region for the conventional multi slope characteristic. At the same time the transient bias increased the differential current operating threshold to A'→B'→C' and enhanced the stability of the differential element.

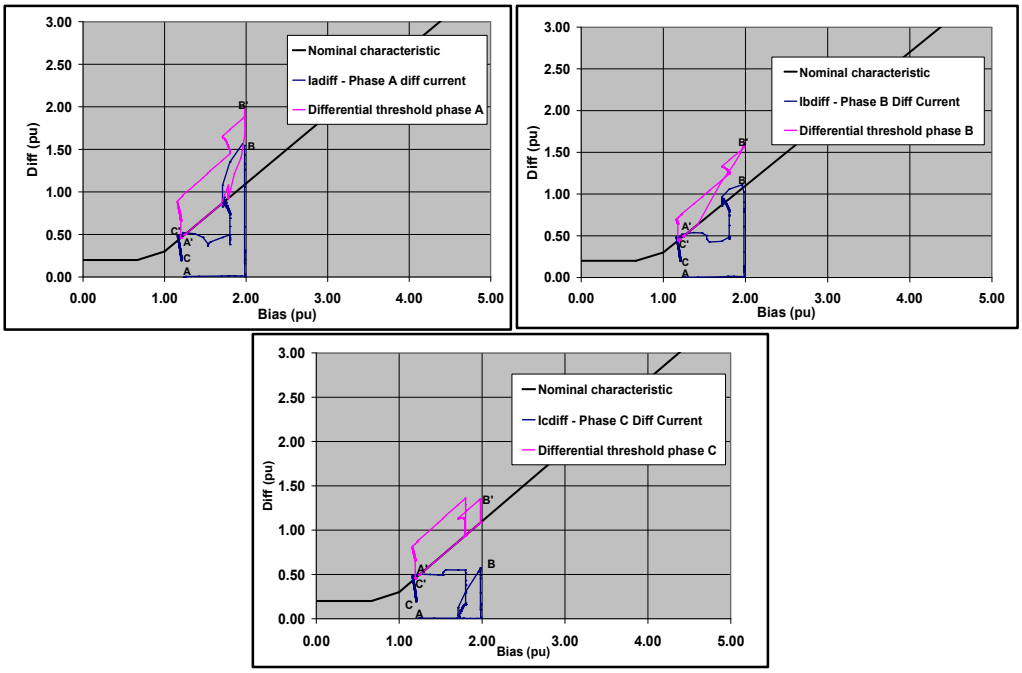

Figure 32 Differential characteristic with transient bias – external fault

4. Field performance analysis with transient bias enabled and disabled

Figure 33 shows details for the differential protection of a 65.3 MVA, 132 kV/13.8 kV transformer. Magnitude and vector compensation in the relay are calculated automatically based on the CT ratio, MVA rating, HV voltage and LV voltage. The full load current of the transformer on the HV and LV side is 285.62 A and 2732.03 A respectively.

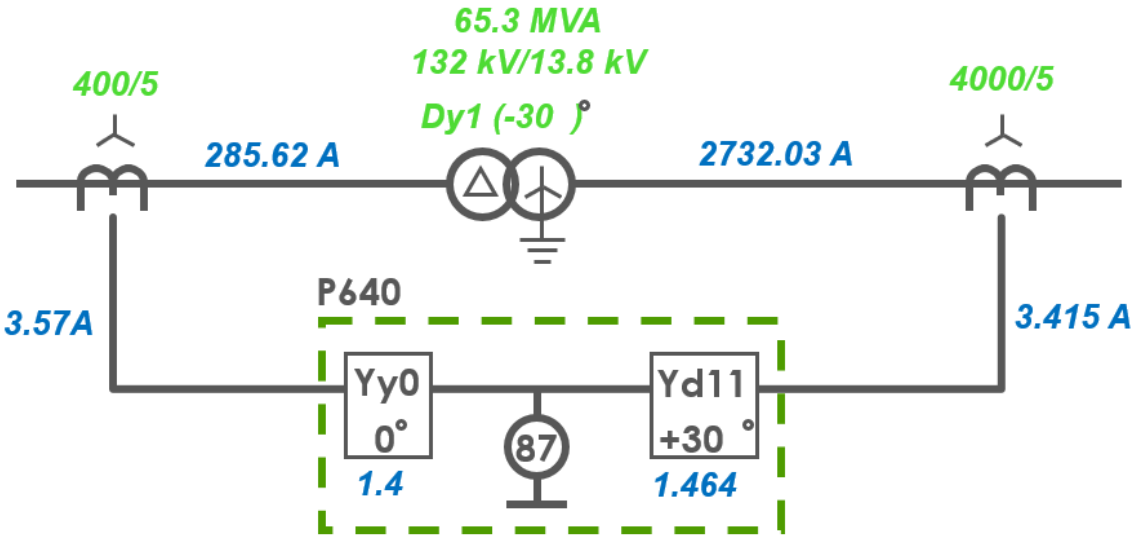

Figure 33 Differential protection using MiCOM P64x

Figure 34 shows the disturbance record for current captured during transformer loading by closing the LV breaker. The energisation of the transformer from the HV breaker was successful and as seen in the record, on closing of the LV breaker an increase in currents is observed on both the HV and LV side simultaneously. It also shows a large difference in the first and second peak of A phase current which could not be due to the primary load current. IN HV in figure 34 is the calculated neutral current and the waveform shows a higher value of neutral current on the HV side which is decaying over time and could be due to CT saturation. For ideal CTs with balanced load on the transformer, the calculated residual current based on IA-1, IB-1 and IC-1 (on Delta side of the transformer) should be zero.

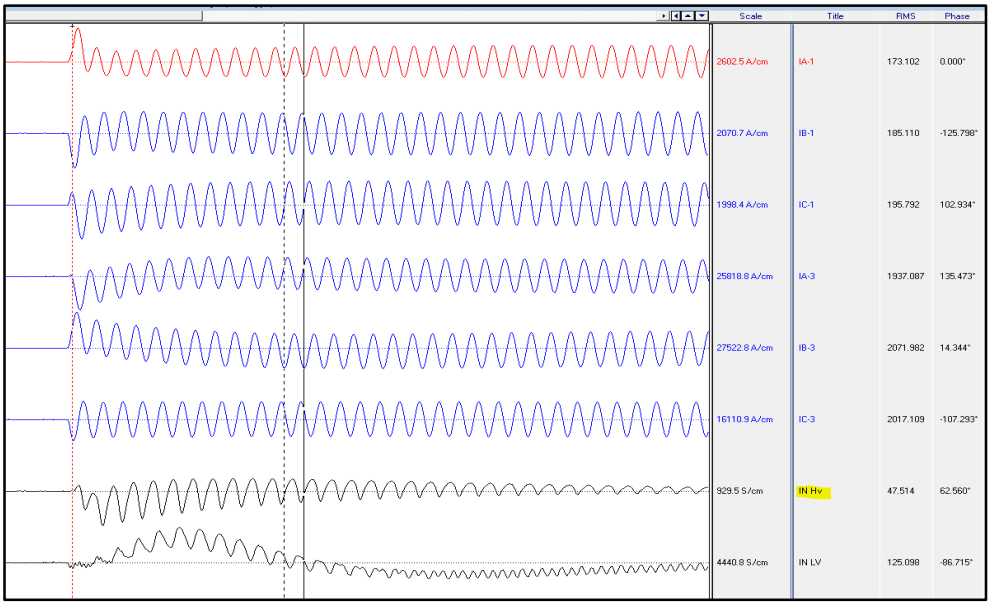

Figure 34 Current captured by relay on LV breaker closing (Transformer loading)

Fig 35 shows the transformer HV and LV current after magnitude and vector compensation. The relay uses these current to calculate the differential and bias currents. Comparing the HV A phase current with the LV A phase current and the HV B phase current with the LV B phase current indicates CT saturation on transformer loading. It could be due to a very high X/R ratio, remanence flux or may be the burden on the CT. Figure 35a shows the operation of the differential elements in A and B phases with the transient bias disabled. Figure 35b shows that the relay remains stable when the transient bias is enabled.

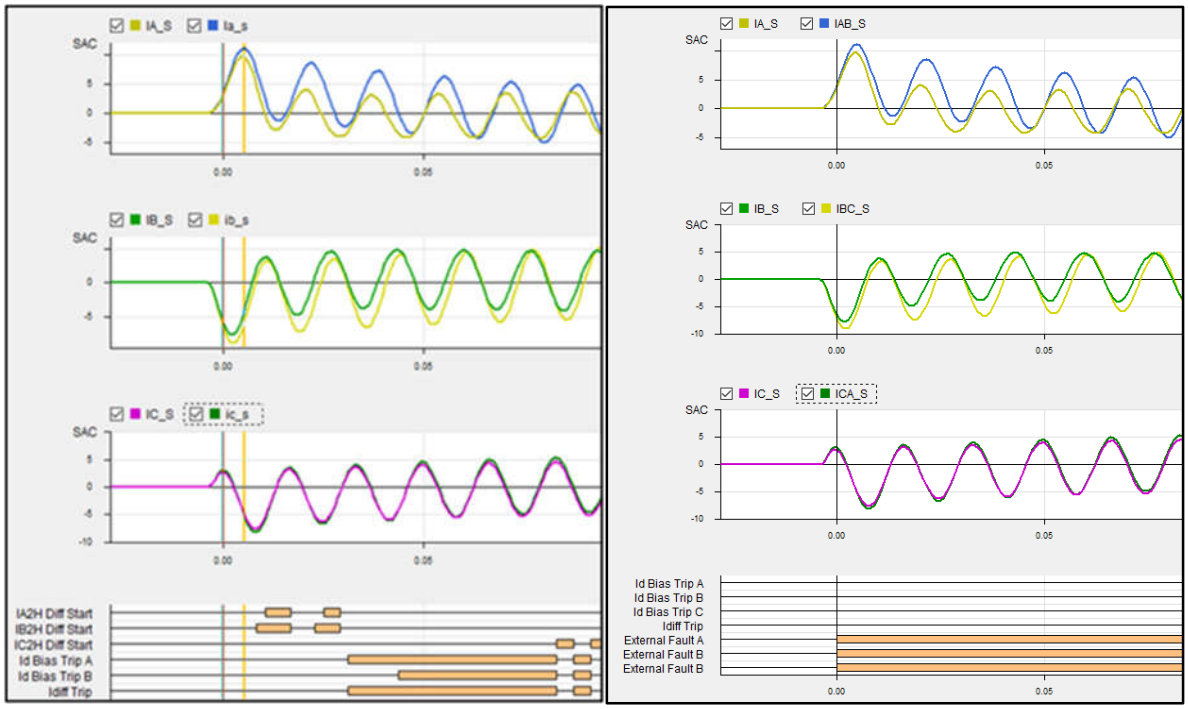

Fig 35a (Transient bias disabled) Fig 35b (Transient bias enabled)

Figure 35 Transformer HV and LV current after magnitude and vector compensation

5. Unblocking of the differential element for faster tripping

There are various methods used to stabilize the transformer differential element during magnetising inrush conditions. The focus of these methods is mainly on blocking or restraining the differential element during magnetising inrush conditions. However, as discussed before internal faults with CT saturation can produce harmonics in the differential current which can slow down the biased differential element. Therefore, it is equally important to unblock the differential element for faster operation during actual internal fault conditions. Unblocking has become even more critical due to the reduction in the threshold of the 2nd harmonic for some newly designed transformers. Figure 36 shows the differential trip logic and unblocking using no gap/CT saturation detection. As seen in the diagram unblocking is only active during internal fault scenarios.

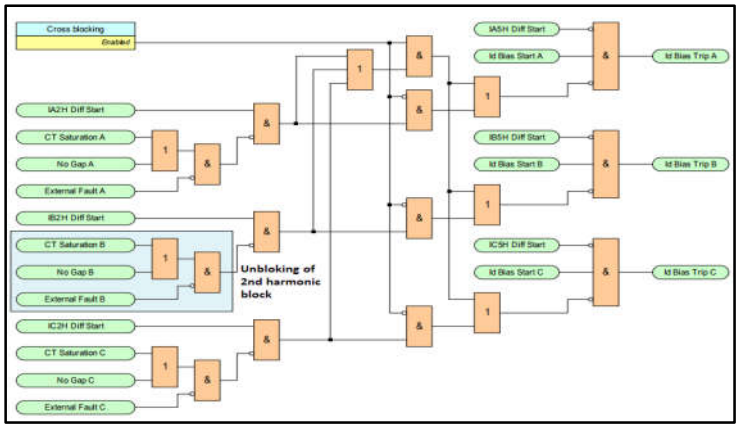

Figure 36 Transformer HV and LV current after magnitude and vector compensation

The no gap detection technique counts the numbers of consecutive samples below a dynamic threshold to determine the low current gap duration in the waveform. The gap is determined on a per phase basis of the differential current and if the gap is less than the defined duration, it considers this as a fault waveform and not an inrush condition. The no gap detection also complements the CT saturation condition during internal faults. Figure 37 shows an example of a 2nd harmonic current generated by a high offset transformer internal fault current. The harmonic bar shows a 2nd harmonic content of 16 % in A phase and 15.8 % in C phase. As the relay is set with a 2nd harmonic blocking threshold of 10%

with cross blocking functionality, without no gap detection it could have resulted in tripping only once the 2nd harmonic goes below the set value. The digital channels show activation of the no gap detection algorithm, indicating this is an internal fault, thus blocking the 2nd harmonic block signal and reducing the operating time for this fault.

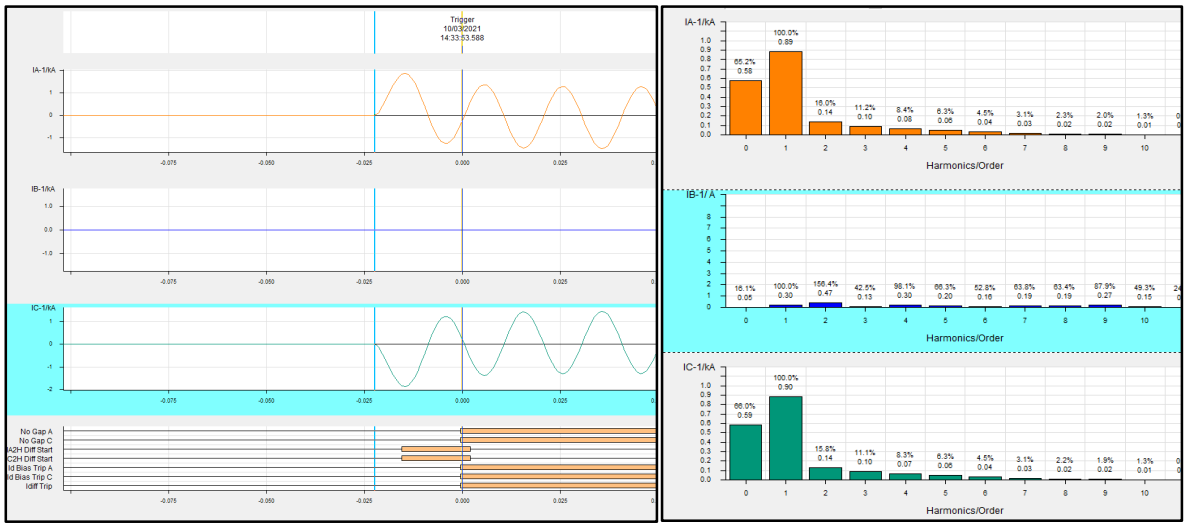

Figure 37 No Gap detection to reduce the operating time in the presence of 2nd harmonic above threshold

Figure 38 shows a fault in one phase during transformer energisation. The record shows a 2nd harmonic of 24.6 % and 11.2 % in B and C phases respectively. As the relay detects a No gap condition in A phase, it unblocks the differential element and releases the trip for faster tripping of the biased differential element.

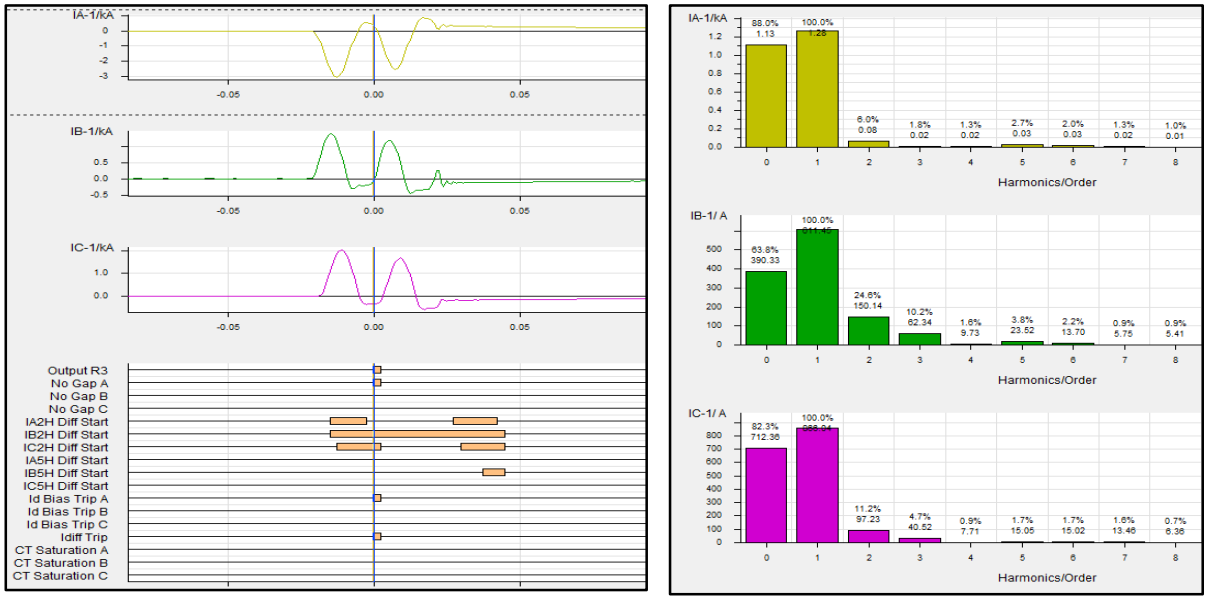

Figure 38 No Gap detection during fault on one phase on transformer energisation

The CT saturation detection technique is a complementary technique to the no gap technique and is used to block 2nd harmonic blocking during internal faults with CT saturation. To detect a CT saturation condition the differential current samples on a per phase basis are considered. The relay analyses the differential current waveforms considering their derivatives dynamically with fixed thresholds determined from RTDS (real time digital simulator) tests.

When a CT saturates, the second harmonic content may be above the second harmonic threshold used for blocking the biased differential protection. As a result, the biased differential element may be blocked

during an internal fault. If the fault level is not high enough for the unrestrained differential element to operate this can result in slow tripping.

Figure 39a is a record of an RTDS test for a phase A-N internal fault and the relay operated in 57 ms when CT saturation and No gap detection is disabled. Figure 39b is the same fault scenario with CT saturation and No gap detection enabled and the operating time is 28 ms.

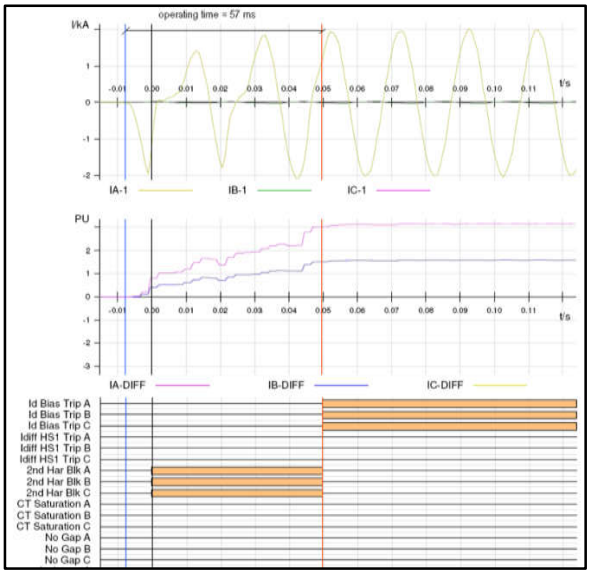

Figure 39a

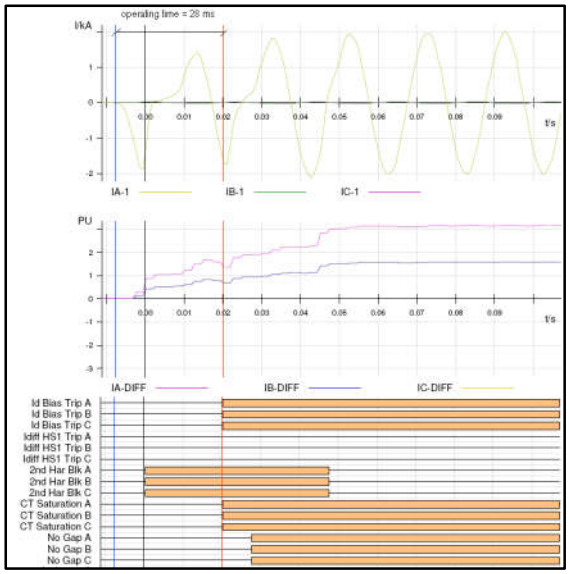

Figure 39b

Figure 39 CT saturation during an internal fault condition

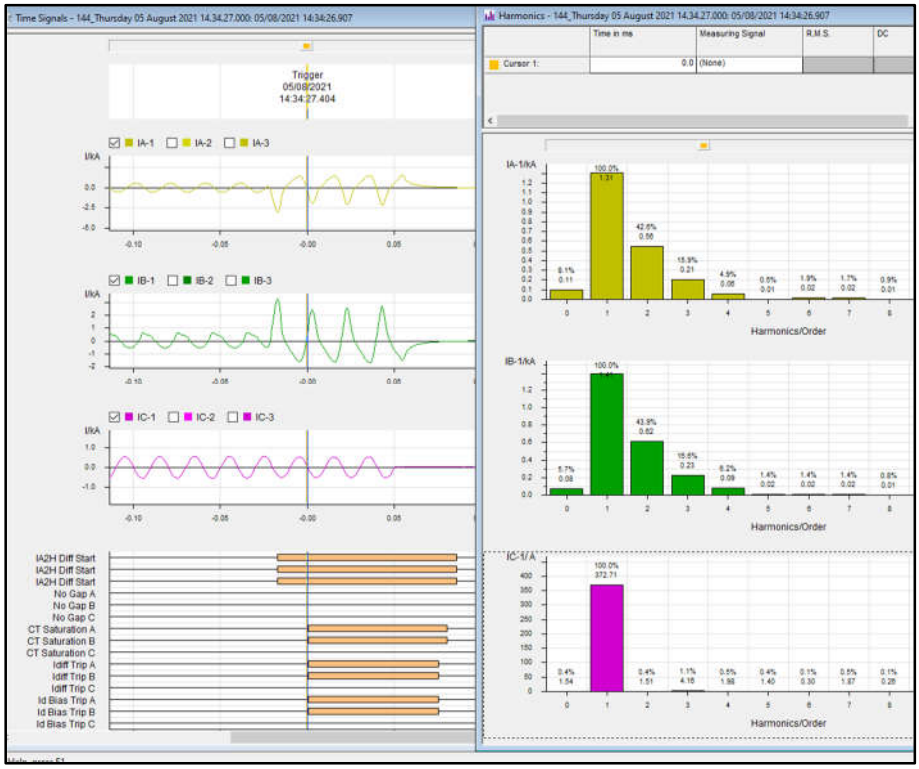

Figure 40 CT saturation during an internal fault condition

Figure 40 shows another example of an RTDS test where the terminal current shows the saturation of the CT during an internal fault. The saturated current waveforms are rich in 2nd harmonic and resulted in activation of the 2nd harmonic blocking signals. It also shows detection of CT saturation during the fault and tripping of the bias differential element in the presence of harmonics.

Figure 41 shows an actual transformer magnetising inrush waveform seen by the relay. It also shows that during the entire magnetising inrush duration, the NO Gap and CT saturation detection were not activated, and energization was successful.

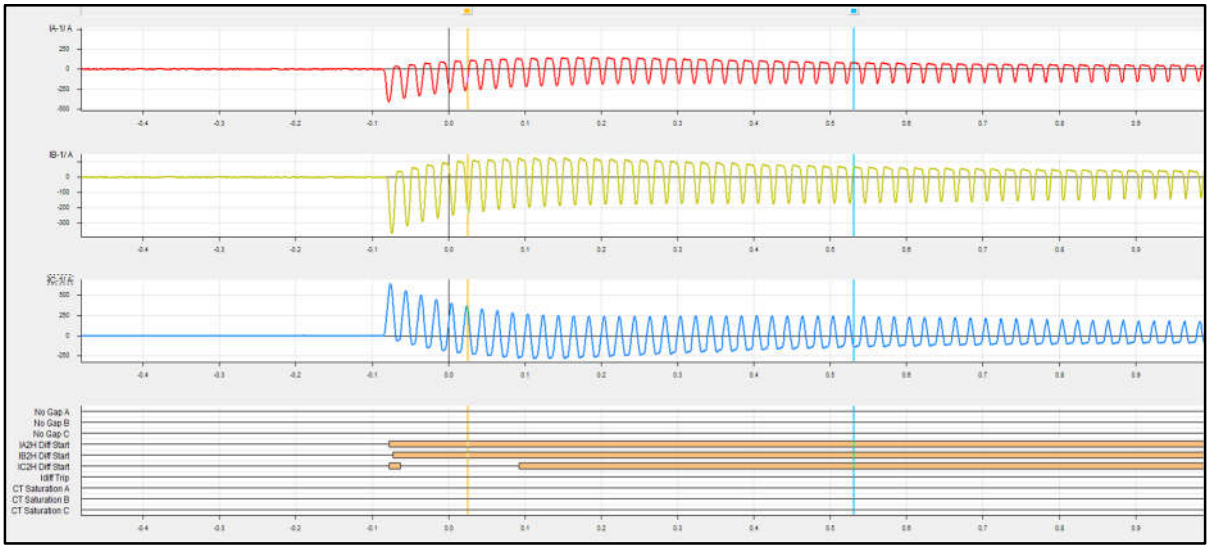

Figure 41 Transformer inrush waveform

6. Conclusion

From the through fault and load cases it is observed that CT saturation causes the differential current locus to move into the operating region. How far it will move into the operating region and when it will come out from operating region (to the restraining region) is dependent upon the level of saturation and the primary & secondary time constants. It also shows that the multi slope characteristic may not be suitable in cases of reduced CT knee point voltage and an additional biasing technique is required. The RTDS test cases and field record show the benefit of the adaptive transient bias algorithm to improve the stability during external fault cases.

The internal fault cases discussed in the paper demonstrate that reducing the CT knee point voltage can cause saturation of the CT's which increases the 2nd harmonics. Higher 2nd harmonics can result in either blocking or delayed tripping of the biased differential element. To overcome this difficulty for faster fault clearance, a method to unblock the biased differential element in presence of CT saturation and higher 2nd harmonics is needed. The CT saturation and no gap waveform recognition techniques reduce the operating time of the biased differential element during such internal faults.

References

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